

R22

Code No: 183AQ

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February - 2024

DIGITAL LOGIC DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours

Max. Marks: 60

Note: This question paper contains two parts A and B.

i) Part- A for 10 marks, ii) Part - B for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of ten questions (numbered from 2 to 11) carrying 10 marks each. From each unit, there are two questions and the student should answer one of them. Hence, the student should answer five questions from Part-B.

PART- A

(10 Marks)

- How many types of parity are there? Name them. [1]
- A bubbled NOR gate is equivalent to which gate? [1]
- What is meant by real minimal expression? [1]
- What are essential prime implicant? [1]
- What is meant Hazards? [1]
- Draw the circuit diagram of Master Slave JK flip flop. [1]
- What is a register? Give applications of it. [1]
- What is a BCD counter? [1]
- Define state Compatibility. [1]
- What is a link path? [1]

PART - B

(50 Marks)

- Express the Decimal Digits 0-9 in BCD, 2421, 84-2-1 and Excess-3.
- Solve for x [5+5]
(i) $(257)_8 = (x)_{10}$ (ii) $(21.625)_{10} = (x)_8$ (iii) $(BC.2)_{16} = (x)_8$ (iv) $(33)_{10} = (201)_x$

OR

- Show that NAND gate and NOR gate are universal gates.
- Detect and correct errors, if any, in the even parity Hamming code words and write the correct code. [5+5]
(i) 1100110 (ii) 0011101 (iii) 0111110

- Simplify the Boolean expression using K-map $F = \bar{A} + AB + AB\bar{D} + A\bar{B}\bar{D} + C$.
- Obtain the minimal expression for $f = \sum(0, 1, 6, 7, 8, 9, 13, 14, 15)$ using the tabular method. [5+5]

OR

- Reduce $\pi M(1, 2, 3, 5, 6, 7, 8, 9, 12, 13)$ using K- map method and implement it in universal logic.
- Realization of AND, OR and NOT Gates Using DTL and TTL logic. [5+5]

6.a) Implement the logic expression given below using a

i) 4:1 MUX ii) 8:1 MUX

$$F = \sum(0, 2, 4, 7).$$

b) Design of a 4-bit gray-to-binary code converter.

[5+5]

OR

7.a) Draw the circuit diagram of a positive edge trigger SR flip-flop and explain its operation with the help of a truth table.

b) Distinguish between combinational and sequential logic circuits.

[5+5]

8. With neat diagrams, explain the working of the following types of left shift registers.

a) Serial-in, Serial-out

b) Parallel-in, Parallel-out

[5+5]

OR

9.a) Implement a 3-bit ripple counter using D flip-flops.

b) Draw and explain the operation of universal shift register.

[5+5]

10.a) What are the capabilities and limitations of finite state machines?

b) For the machine given in Table, find the equivalence partition and a corresponding reduced machine in standard form and also explain the procedure.

[5+5]

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

OR

11.a) Explain the procedure of state minimization using the merger graph and merger table.

b) Name the element of an ASM chart and a conventional flow chart.

[5+5]

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